PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference AD001	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/IL2004/001055	International filing date *(day/month/year)* 17 November 2004 (17.11.2004)	Priority date *(day/month/year)* 11 December 2003 (11.12.2003)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant ADVASENSE TECHNOLOGICS (2004) LTD.		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 10 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☒	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☒	Box No. VII	Certain defects in the international application
☒	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 12 June 2006 (12.06.2006)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Simin Baharlou
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Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
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WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing (*day/month/year*)	27 OCT 2005
Applicant's or agent's file reference AD001	FOR FURTHER ACTION See paragraph 2 below

International application No.	International filing date (*day/month/year*)	Priority date (*day/month/year*)
PCT/IL04/01055	17 November 2004 (17.11.2004)	11 December 2003 (11.12.2003)

International Patent Classification (IPC) or both national classification and IPC

IPC(7): H04N 5/217, 3/14, 5/335; H01L 27/00 and US Cl.: 348/241, 308; 250/208.1

Applicant

ADVASENSE TECHNOLOGIES LTD.

1. This opinion contains indications relating to the following items:

☒	Box No. I	Basis of the opinion
☒	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☒	Box No. VII	Certain defects in the international application
☒	Box No. VIII	Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(*b*) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/ US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Authorized officer Wendy Garber Telephone No. (703) 305-9600

Form PCT/ISA/237 (cover sheet) (January 2004)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/IL04/01055

Box No. I Basis of this opinion

1. With regard to the language, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

☐ This opinion has been established on the basis of a translation from the original language into the following language _____, which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).

2. With regard to any nucleotide and/or amino acid sequence disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

a. type of material

☐ a sequence listing

☐ table(s) related to the sequence listing

b. format of material

☐ in written format

☐ in computer readable form

c. time of filing/furnishing

☐ contained in international application as filed.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/IL04/01055

Box No. II Priority

1. ☐ The following document has not yet been furnished:

   ☐ copy of the earlier application whose priority has been claimed (Rules 43*bis*.1 and 66.7(a)).

   ☐ translation of the earlier application whose priority has been claimed (Rules 43*bis*.1 and 66.7(b)).

   Consequently it has not been possible to consider the validity of the priority claim. This opinion has nevertheless been established on the assumption that the relevant date is the claimed priority date.

2. ☒ This opinion has been established as if no priority has been claimed due to the fact that the priority claim has been found invalid (Rules 43*bis*.1 and 64.1). Thus for the purposes of this opinion, the international filing date indicated above is considered to be the relevant date.

3. Additional observations, if necessary:
   The priority claim is considered invalid because none of the claims are supported by the priority application.

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/IL04/01055

Box No. V Reasoned statement under Rule 43 *bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims 4, 5, 20	YES
	Claims 1-3, 6-19, 21-37	NO
Inventive step (IS)	Claims 4, 5, 20	YES
	Claims 1-3, 6-19, 21-37	NO
Industrial applicability (IA)	Claims 1-37	YES
	Claims NONE	NO

2. Citations and explanations:

Please See Continuation Sheet

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/IL04/01055

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

The drawings are objected to under PCT Rule 66.2(a)(iii) as containing the following defect(s) in the form or content thereof:
In Figure 1, applicant does not disclose a reference number 19, which is discussed in the specification.
In Figure 2 there is no reference number 20' as mentioned in the specification.
In Figure 3 there are not reference numbers 10', 20", or I3 as mentioned in the specification.

The description is objected to as containing the following defect(s) under PCT Rule 66.2(a)(iii) in the form or contents thereof:
In page 5, paragraph 0027 applicant refers to reference number M5 45 as being the PMOS transistor. However it is clear from the drawings that the second current source is the PMOS transistor, M5 42.
In page 6, paragraph 0031 applicant refers to reference number 32 as being the current mirror in Figure 3. However, it is clear from an analysis of Figure 3 that the current mirror is actually reference number 35.

Claim 17 is objected to under PCT Rule 66.2(a)(iii) as containing the following defect(s) in the form or contents thereof:
In line 2 of claim 17, applicant recites the phrase "at least one current sources". This appears to be a typographical error and that the applicant meant to use the phrase - at least one current source -.

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/IL04/01055

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the questions whether the claims are fully supported by the description, are made:

Claim 5 is objected to under PCT Rule 66.2(a)(v) as lacking clarity under PCT Article 6 because claim 5 is indefinite for the following reason(s): Claim 5 recites the limitation "the at least one current mirror". This limitation lacks antecedent basis since the limitation was never mentioned previously in claim 5 or in the parent claim, claim 1. Therefore, the limitation "the at least one current mirror" is indefinite.

Supplemental Box
In case the space in any of the preceding boxes is not sufficient.

V. 2. Citations and Explanations:

1. Claims 1, 2, 6-11, 14, 16-19, 21-31, 33, 34, and 37 lack novelty under PCT Article 33(2) as being anticipated by Kozlowski et al. (U.S. Patent No. 6,587,142).
2. Regarding ***claim 1***, Kozlowski discloses a low-noise active-pixel sensor (APS) with a high speed reset. The APS includes a pixel (10) which receives light and outputs a current representative of the received light. Additionally, Kozlowski discloses the use of feedback circuitry in the form of the current source (30), the amplifier (40), and the bus (101). The amplifier receives the current from the pixel (10) and a reference current (REF) to provide a feedback signal to the pixel (10) during a reset stage. See Figures 5 and 6, and column 7, line 5 to column 10, line 40.
3. As for ***claim 2***, Kozlowski discloses that the feedback circuitry includes an amplifier (40).
4. With regard to ***claim 6***, Kozlowski discloses that he pixel includes three transistors (M1, M2, and M3) and a light sensitive element (photodiode, 12).
5. Regarding ***claim 7***, Kozlowski discloses that the APS is composed of several pixels, wherein each of the pixels is coupled to the feedback circuitry. See column 7, lines 4-37 and Figure 3.
6. As for ***claim 8***, the capacitor, C_{store}, serves as the analog memory for storing analog signals of previously received light. See column 8, lines 40-55.
7. With regard to ***claim 9***, as mentioned in column 8, lines 40-55, Kozlowski discloses that the reset signal value is responsive to a previous pixel output signal.
8. Regarding ***claim 10***, Kozlowski discloses a low-noise active-pixel sensor (APS) with a high speed reset. The APS includes a pixel (10) which receives light and outputs a current representative of the received light. Additionally, Kozlowski discloses the use of feedback circuitry in the form of the current source (30), the amplifier (40), and the bus (101). The amplifier receives the current from the pixel (10) and a reference current (REF) to provide a feedback signal to the pixel (10) during a reset stage. See Figures 5 and 6, and column 7, line 5 to column 10, line 40. Furthermore, multiple feedback signals are provided to the pixel during the reset stage, since a new feedback signal is sent during each different reset stage. See Figures 5 and 6.
9. As for ***claim 11***, the first feedback signal is the feedback signal provided during a first reset stage and the second feedback signal is the feedback signal provided during a second reset stage.
10. With regard to ***claims 14 and 37***, since the feedback loops are provided to each of the pixels in the APS array, there are inherently multiple feedback loops.
11. Regarding ***claim 16***, Kozlowski discloses the use of an amplifier (40) used in the feedback circuitry.
12. As for ***claim 17***, Kozlowski discloses the use of a current source (30) in the feedback loop.
13. With regard to ***claim 18***, Kozlowski discloses that he pixel includes three transistors (M1, M2, and M3) and a light sensitive element (photodiode, 12).
14. Regarding ***claim 19***, Kozlowski discloses that the APS is composed of several pixels, wherein each of the pixels is coupled to the feedback circuitry. See column 7, lines 4-37 and Figure 3.
15. As for ***claim 21***, the capacitor, C_{store}, serves as the analog memory for storing analog signals of previously received light. See column 8, lines 40-55.
16. With regard to ***claim 22***, as mentioned in column 8, lines 40-55, Kozlowski discloses that the reset signal value is responsive to a previous pixel output signal.
17. Regarding ***claim 23***, Kozlowski discloses a low-noise active-pixel sensor (APS) with a high speed reset. The APS array includes a plurality of pixels (10) which receives light and outputs a current representative of the received light. Additionally, Kozlowski

Supplemental Box
In case the space in any of the preceding boxes is not sufficient.

discloses the use of feedback circuitry in the form of the current source (30), the amplifier (40), and the bus (101). The amplifier receives the current from the pixel (10) and a reference current (REF) to provide a feedback signal to the pixel (10) during a reset stage. See Figures 5 and 6, and column 7, line 5 to column 10, line 40. Furthermore, multiple feedback signals are provided to the pixel during the reset stage, since a new feedback signal is sent during each different reset stage. See Figures 5 and 6.

18. As for *claim 24*, Kozlowski discloses that each row of pixels is coupled to the feedback circuitry. Each row of pixels has at least one pixel connected to the feedback circuitry.

19. With regard to *claim 25*, Kozlowski discloses that each column of pixels is coupled to the feedback circuitry. As discussed in column 7, lines 15-18, the video buss (20) connects each pixel in a column to the feedback circuitry.

20. *Claim 26* is considered substantively equivalent to claim 23. Please see the discussion of claim 23 above.

21. *Claim 27* is considered a method claim corresponding to claim 1. Please see the discussion of claim 1 above.

22. *Claim 28* is considered a method claim corresponding to claim 7. Please see the discussion of claim 7 above.

23. *Claim 29* is considered a method claim corresponding to claim 8. Please see the discussion of claim 8 above.

24. As for *claim 30*, the amplifier (40) serves as the means for generating the feedback signal.

25. With regard to *claim 31*, the amplifier generates the feedback signal by a difference between the pixel current and a reference current (REF). See Figure 3.

26. *Claim 33* is considered a method claim corresponding to claim 10. Please see the discussion of claim 10 above.

27. *Claim 34* is considered a method claim corresponding to claim 11. Please see the discussion of claim 11 above.

28. Claims 1-3, 6-16, 18, 19, and 21-37 lack novelty under PCT Article 33(2) as being anticipated by Lee (U.S. Patent No. 6,777,660).

29. Regarding *claim 1*, Lee discloses a CMOS APS image sensor capable of reducing the noise during reset. More specifically, Lee discloses a pixel (31) for receiving light and outputting a current representative of the light and feedback circuitry comprised of the amplifier (33) and the bus. During reset, the amplifier (33) feedsback a signal to the reset transistor (45) to reduce the reset noise.

30. As for *claim 2*, Lee discloses that the feedback circuitry includes an amplifier (33).

31. With regard to *claim 3*, Lee discloses that the amplifier (33) includes a current mirror comprised of the transistors M4A and M5A. See Figure 5 and column 6, lines 28-30.

32. Regarding *claim 6*, Lee discloses that the pixel includes three transistors (M1, M2, and M3) and a light sensitive element (photodiode, see abstract).

33. As for *claim 7*, Figure 4a shows that the image sensor is comprised of multiple pixels (31) and coupling circuitry for selectively coupling the pixel to the feedback circuitry.

34. With regard to *claim 8*, Figure 2 shows the use of a capacitor (C, 50) for storing analog signals of previously received light.

35. Regarding *claim 9*, as discussed in the abstract and column 4, line 35 to column 5, line 65, the reset value supplied to the reset transistor is responsive to the previous pixel output signal.

36. Regarding *claim 10*, Lee discloses a CMOS APS image sensor capable of reducing the noise during reset. More specifically, Lee discloses a pixel (31) for receiving light and outputting a current representative of the light and feedback circuitry comprised of the amplifier (33) and the bus. During reset, the amplifier (33) feedsback a signal to the reset transistor (45) to reduce the reset noise. Furthermore, multiple feedback signals are provided to the pixel during the reset stage, since a new feedback signal is sent during each different reset stage.

37. As for *claim 11*, the first feedback signal is the feedback signal provided during a first reset stage and the second feedback signal is the feedback signal provided during a second reset stage.

38. With regard to *claim 12*, the feedback signal provided during the first reset stage affects a reset voltage supplied to the pixel (31). See the abstract and column 4, line 35 to column 5, line 65.

39. Regarding *claim 13*, the feedback signal provided during the second reset stage contributes to a reduction of a capacitance that contributes to a thermal noise of a the pixel. See column 5, lines 3-14.

40. As for *claims 14 and 37*, since the feedback loops are provided to each of the pixels in the APS array, there are multiple feedback loops - one to each pixel. See Figures 4a and 4b.

41. With regard to *claim 15*, Lee discloses that the amplifier (33) includes a current mirror comprised of the transistors M4A and M5A. See Figure 5 and column 6, lines 28-30.

42. Regarding *claim 16*, Lee discloses that the feedback circuitry includes an amplifier (33).

43. As for *claim 18*, Lee discloses that the pixel includes three transistors (M1, M2, and M3) and a light sensitive element (photodiode, see abstract).

44. With regard to *claim 19*, Figure 4a shows that the image sensor is comprised of multiple pixels (31) and coupling circuitry for selectively coupling the pixel to the feedback circuitry.

45. Regarding *claim 21*, Figure 2 shows the use of a capacitor (C, 50) for storing analog signals of previously received light.

46. As for *claim 22*, as discussed in the abstract and column 4, line 35 to column 5, line 65, the reset value supplied to the reset transistor is responsive to the previous pixel output signal.

47. With regard to *claim 23*, Lee discloses a CMOS APS image sensor capable of reducing the noise during reset. More specifically, Lee discloses a plurality of pixels (31) for receiving light and outputting a current representative of the light and feedback circuitry comprised of the amplifier (33) and the bus. During reset, the amplifier (33) feedsback a signal to the reset transistor (45) to reduce the reset noise. Furthermore, multiple feedback signals are provided to the pixel during the reset stage, since a new feedback signal is sent during each different reset stage. See Figure 4a and 4b.

48. Regarding *claim 24*, Lee discloses that each row is connected to the same feedback circuitry in Figure 4b.

49. As for *claim 25*, Lee discloses that each row is connected to the same feedback circuitry in Figure 4a.

International application No.
PCT/IL04/01055

Supplemental Box
In case the space in any of the preceding boxes is not sufficient.

50. *Claim 26* is considered substantively equivalent to claim 23. Please see the discussion of claim 23 above.
51. *Claim 27* is considered a method claim corresponding to claim 1. Please see the discussion of claim 1 above.
52. *Claim 28* is considered a method claim corresponding to claim 7. Please see the discussion of claim 7 above.
53. *Claim 29* is considered a method claim corresponding to claim 8. Please see the discussion of claim 8 above.
54. As for *claim 30*, the amplifier (33) serves as the means for generating the feedback signal.
55. With regard to *claim 31*, the amplifier generates the feedback signal by a difference between the pixel current and a reference current (Vr). See Figure 4a.
56. Regarding *claim 32*, Lee discloses that the amplifier (33) includes a current mirror comprised of the transistors M4A and M5A. See Figure 5 and column 6, lines 28-30.
57. *Claim 33* is considered a method claim corresponding to claim 10. Please see the discussion of claim 10 above.
58. *Claim 34* is considered a method claim corresponding to claim 11. Please see the discussion of claim 11 above.
59. *Claim 35* is considered a method claim corresponding to claim 12. Please see the discussion of claim 12 above.
Claim 36 is considered a method claim corresponding to claim 13. Please see the discussion of claim 13 above.